2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. Of: SAEKI

Serial No.: 09/910,117

Filed: July 20, 2001

For: CLOCK CONTROLLING METHOD AND CIRCUIT

Group: 2816

Examiner: LINH M. NGUYEN DOCKET: NEC G226

#14 Response 6/28/03

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT D

Dear Sir:

This Amendment is being filed in response to the Official Action mailed March 14, 2003.

REMARKS

The allowance of claims 33-35 is noted, with thanks.

Turning to the Examiner's rejection of claims 1, 28 and 31 under 35 USC § 102(e) as anticipated by Takemae et al. (U.S. Patent 6,194,932), the Examiner's rejection is in error. Claims 1, 28 and 31 require that the phase be adjusted by a predetermined unit value of a phase differential on each clock cycle of the referenced clock. Takemae et al. does not teach this feature. As shown by the timing chart of Takemae et al., each clock cycle of what the Examiner is calling the referenced clock, or clock zero, is only shifted once upon the output clock signal and form (Fig. 2; Fig. 3). However, in the instant claimed invention, as shown, e.g., in Fig. 2, each cycle of the clock is shifted by a predetermined amount causing an increase in the phase shift after each cycle as can be shown by the exemplary shift $\Delta\Phi$, $2\Delta\Phi$, and $3\Delta\Phi$. Thus,

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